ABSTRACT OF THE DISCLOSURE

A method for fabricating a non-volatile memory is described. A substrate having a strip stacked structure thereon is provided. A buried drain is then formed in the substrate beside the strip stacked structure and an insulating layer is formed on the buried drain. A silicon layer and a cap layer are sequentially formed over the substrate. The cap layer, the silicon layer and the strip stacked structure are then patterned successively in a direction perpendicular to the buried drain, wherein the strip stacked structure is patterned into a plurality of gates. A liner oxide layer is formed on the exposed surfaces of the gates, the substrate and the silicon layer. Thereafter, the cap layer is removed and a metal salicide layer is formed on the exposed surface of the silicon layer.